What is claimed is:

1. A method for performing timing recovery comprising:

producing phase signals by comparing a signal received at each of a plurality of inputs to a timing signal produced by a numerically controlled oscillator (NCO);

summing said phase signals to produce a sum;

adjusting said sum into an input range for the numerically controlled oscillator (NCO); and

producing a timing signal within the NCO in response to the adjusted sum.

2. The method of claim 1 wherein said adjusting comprises:
determining whether each input can be accurately received; and
dividing the sum by a number of potentially receivable inputs.

3. The method of claim 2 wherein said determining comprises:

determining whether an amplitude of each input is greater than a threshold value.

4. The method of claim 1 wherein said adjusting comprises:
determining whether each input is receivable;
determining an offset using a number of receivable inputs; and
adjusting the sum using the offset.

5. The method of claim 4 wherein said determining comprises:
determining whether an amplitude of each input is above a threshold value.

6. The method of claim 4 wherein said adjusting by said offset comprises:
adding the sum by the offset if the sum is below the input range.

7. The method of claim 4 wherein said adjusting by said offset comprises: subtracting the sum by the offset if the sum is above the input range.

8. An apparatus for performing timing recovery of a signal received at a plurality of inputs, said apparatus comprising:

a plurality of phase detectors each detecting a phase of said signal at a different input by comparing the input signal to a timing signal from a numerically controlled oscillator (NCO);

a summer for adding said detected phases to form a sum;

a level shifter for adjusting the sum to within an input range of said NCO;

a loop filter for filtering the adjusted sum; and

the NCO for generating a timing signal in response to the filtered sum.

9. The apparatus of claim 8 further comprising:

a plurality of signal detectors each for determining whether an input signal is receivable; and

a decision circuit using a total of receivable input signals to determine an adjustment to the sum by said level shifter.

10. The apparatus of claim 9 wherein said decision circuit divides the sum by the total of receivable input signals.

11. The apparatus of claim 9 wherein said decision circuit determines an offset that is added to or subtracted from the sum by said level shifter.